FAIRCHILD

SEMICONDUCTOR®

FDMS8660AS

N-Channel PowerTrench® SyncFET™

30V, 49A, 2.1mΩ

Features

- Max $r_{DS(on)}$ = 2.1mΩ at V_{GS} = 10V, I_D = 28A

- Max $r_{DS(on)}$ = 3.1mΩ at V_{GS} = 4.5V, I_D = 22A

- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency

- SyncFET Schottky Body Diode

- MSL1 robust package design

- RoHS Compliant

General Description

The FDMS8660AS has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

Applications

- Synchronous Rectifier for DC/DC Converters

- Notebook Vcore/ GPU low side switch

- Networking Point of Load low side switch

- Telecom secondary side rectification

Power 56 (Bottom view)
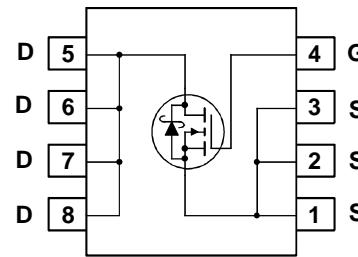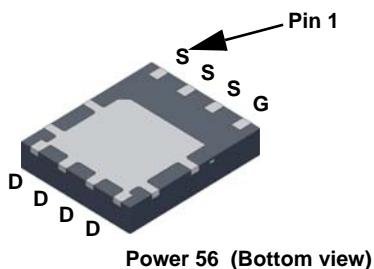
MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			30	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25°C		49	A
	-Continuous (Silicon limited)	T_C = 25°C		179	
	-Continuous	T_A = 25°C	(Note 1a)	28	
	-Pulsed			200	
E_{AS}	Single Pulse Avalanche Energy		(Note 2)	726	mJ
P_D	Power Dissipation	T_C = 25°C		104	W
	Power Dissipation	T_A = 25°C	(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

			Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8660AS	FDMS8660AS	Power 56	13''	12mm	3000units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1mA, V_{GS} = 0V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 10mA, referenced to 25°C		27		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V			500	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1mA	1.0	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 10mA, referenced to 25°C		-5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 28A		1.7	2.1	mΩ
		V_{GS} = 4.5V, I_D = 22A		2.3	3.1	
		V_{GS} = 10V, I_D = 28A, T_J = 125°C		2.3	3.1	
g_{FS}	Forward Transconductance	V_{DD} = 10V, I_D = 28A		167		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		4410	5865	pF
C_{oss}	Output Capacitance			2305	3065	pF
C_{rss}	Reverse Transfer Capacitance			185	280	pF
R_g	Gate Resistance	f = 1MHz		1.2		Ω

Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15V, I_D = 28A, V_{GS} = 10V, R_{GEN} = 6Ω		16	29	ns
t_r	Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			42	68	ns
t_f	Fall Time			5	10	ns
Q_g	Total Gate Charge	V_{GS} = 0V to 10V	V_{DD} = 15V, I_D = 28A	59	83	nC
Q_g	Total Gate Charge	V_{GS} = 0V to 4.5V		30	42	nC
Q_{gs}	Gate to Source Charge			12		nC
Q_{gd}	Gate to Drain "Miller" Charge			5.2		nC

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S =2A (Note 3)		0.4	0.7	V
t_{rr}	Reverse Recovery Time	I_F = 28A, di/dt = 300A/µs		46	74	ns
Q_{rr}	Reverse Recovery Charge			67	108	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a. 50°C/W when mounted on a 1 in² pad of 2 oz copper.

b. 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Starting T_J = 25°C, L = 3mH, I_{AS} = 22A, V_{DD} = 30V, V_{GS} = 10V.

3. Pulse Test: Pulse Width < 300µs, Duty cycle < 2.0%.

Typical Characteristics T_J = 25°C unless otherwise noted
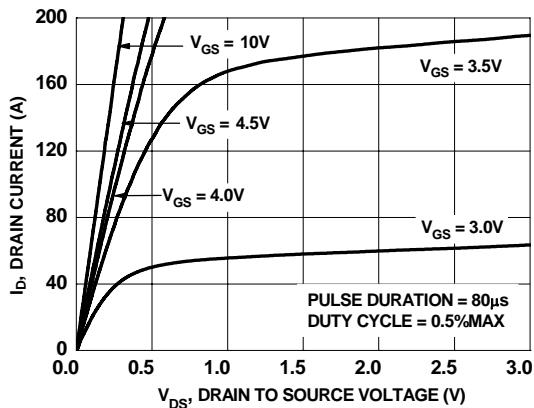

Figure 1. On-Region Characteristics
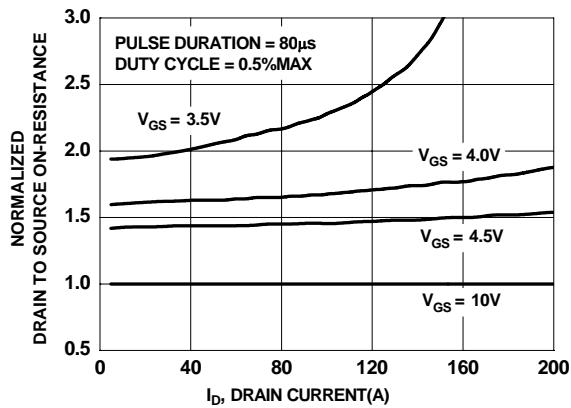
Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage
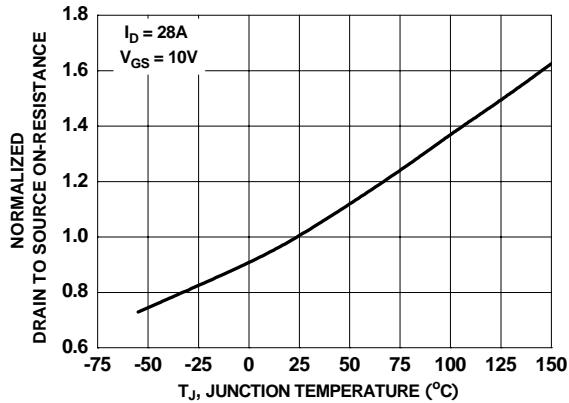
Figure 3. Normalized On-Resistance vs Junction Temperature
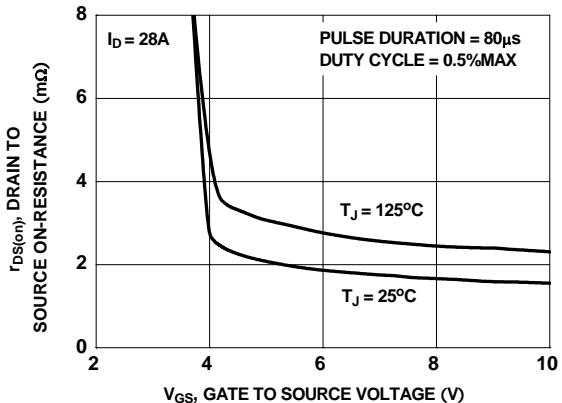

Figure 4. On-Resistance vs Gate to Source Voltage
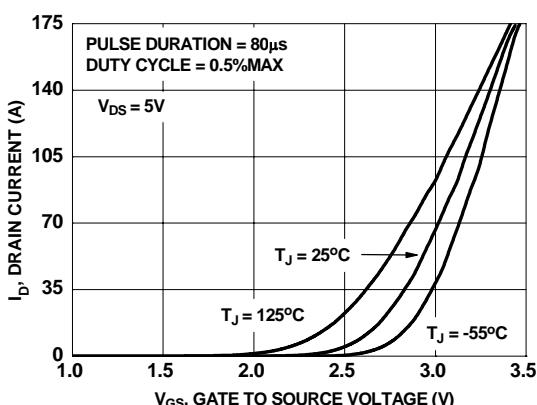
Figure 5. Transfer Characteristics
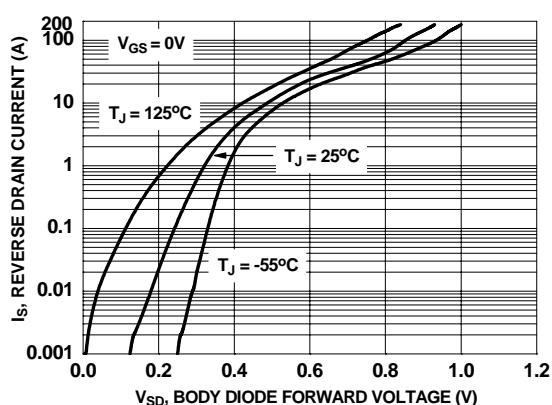

Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## Typical Characteristics $T_J = 25°C$ unless otherwise noted
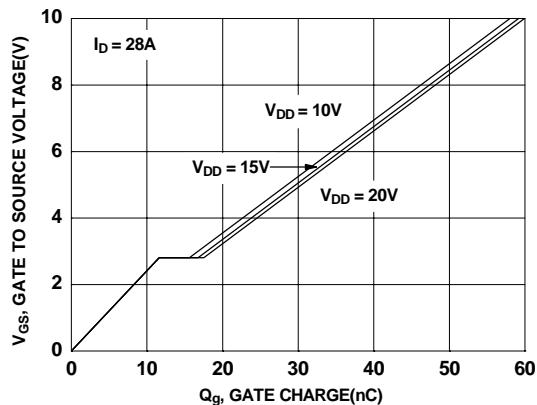
**Figure 7. Gate Charge Characteristics**
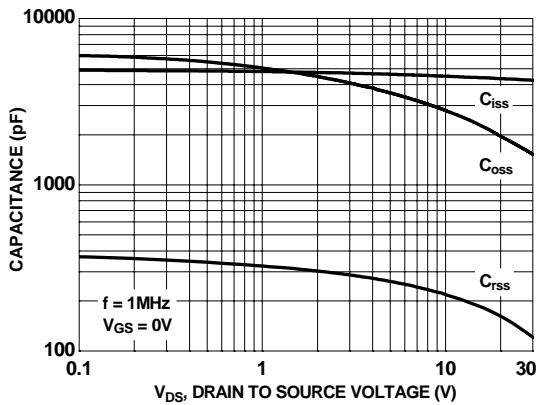
**Figure 8. Capacitance vs Drain to Source Voltage**
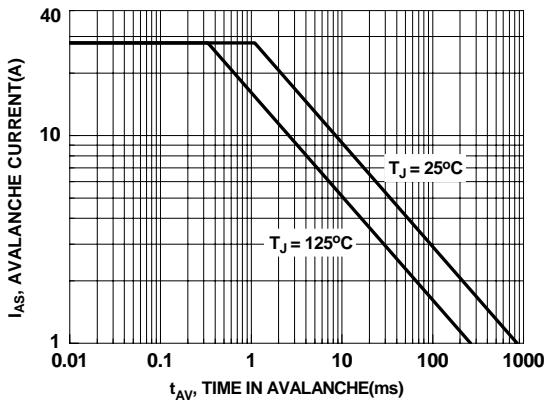
**Figure 9. Unclamped Inductive Switching Capability**
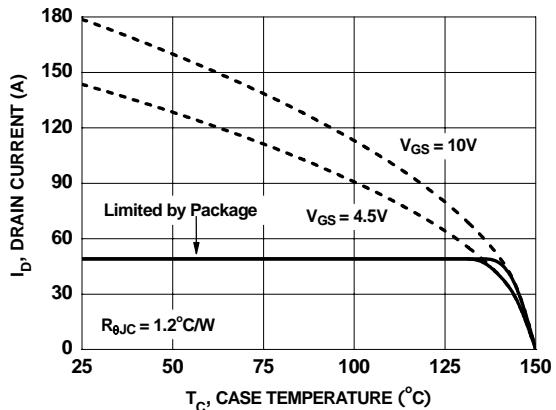
Figure 10. Maximum Continuous Drain Current vs Case Temperature
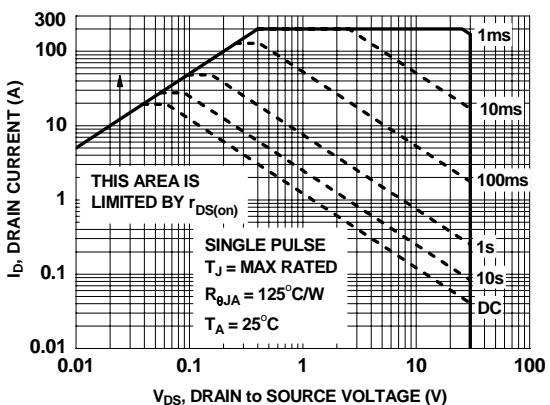
Figure 11. Forward Bias Safe Operating Area
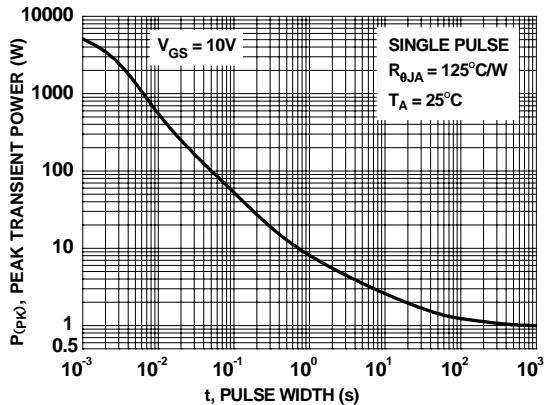
Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25°C$ unless otherwise noted
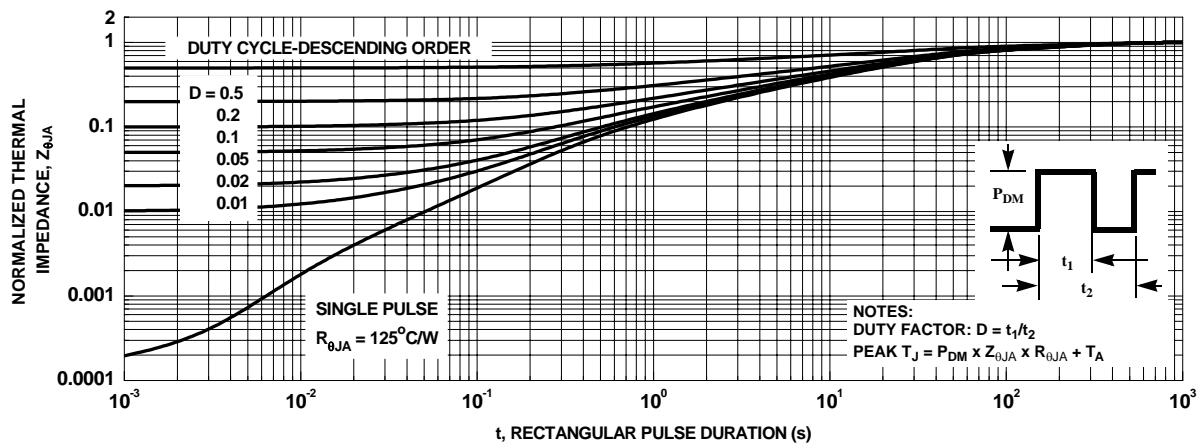
Figure 13. Transient Thermal Response Curve

The graph shows:
- Y-axis: NORMALIZED THERMAL IMPEDANCE, $Z_{\theta JA}$ (0.0001 to 2)
- X-axis: t, RECTANGULAR PULSE DURATION (s) (10^{-3} to 10^3)
- DUTY CYCLE-DESCENDING ORDER
- D = 0.5, 0.2, 0.1, 0.05, 0.02, 0.01
- SINGLE PULSE
- $R_{\theta JA} = 125°C/W$

NOTES:
DUTY FACTOR: $D = t_1/t_2$
PEAK $T_J = P_{DM}$ x $Z_{\theta JA}$ x $R_{\theta JA} + T_A$

Typical Characteristics (continued)

SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS8660AS.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.
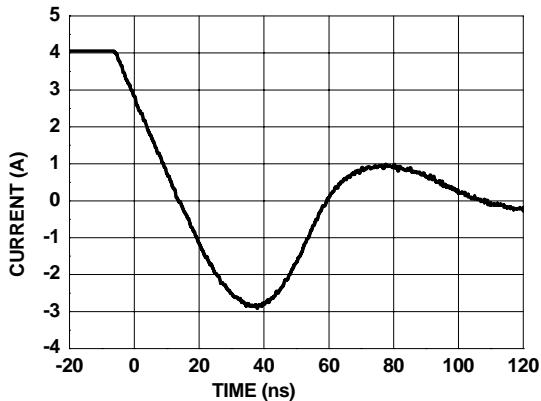
Figure 14. FDMS8660AS SyncFET Body Diode Reverse Recovery Characteristics
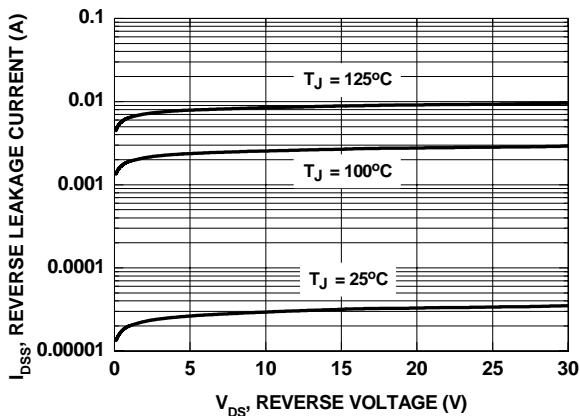
Figure 15. SyncFET Body Diode Reverse Leakage vs Drain to Source Voltage

5.00 [A]

PKG ℄

8   5   [B]

PKG ℄   6.00

PIN #1
INDICATOR   1   4
TOP VIEW

3.91   1.27

8 7 6 5
0.77

4.52   6.61

1.27

1 2 3 4

1.27   0.61
3.81

LAND PATTERN
RECOMMENDATION

1.05
// 0.10 C
⌓ 0.08 C

0.06
0.00

SIDE VIEW   C

3.81
1.27

(0.39)   0.46
0.36

1 2 3 4   ⊕ 0.10Ⓜ C A B

0.64
0.44

PIN #1
IDENT
(OPTIONAL)   (0.35)

1.81   4.01±0.30

0.64
0.44

8 7 6 5

3.86
3.66
BOTTOM VIEW
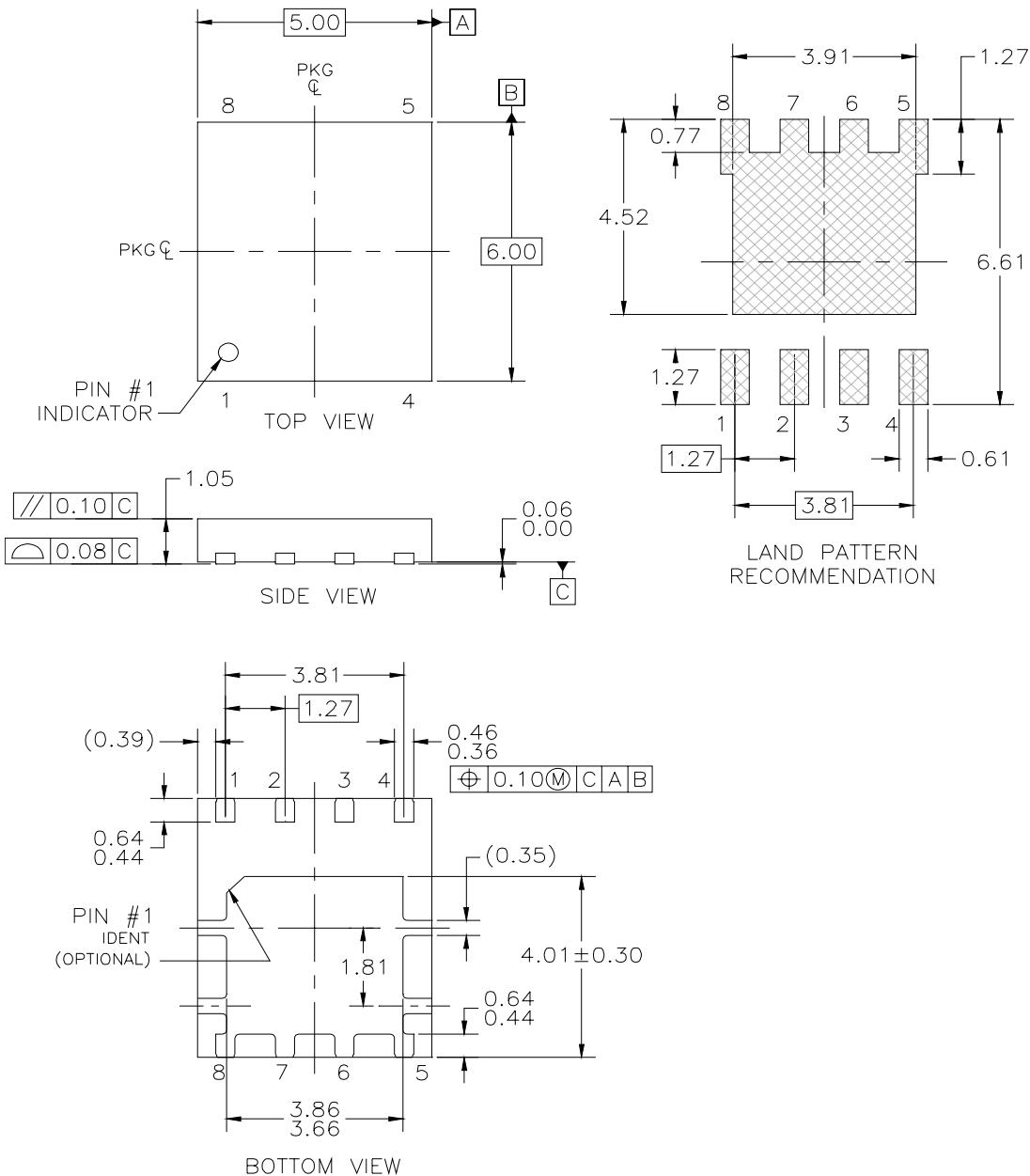
NOTES: UNLESS OTHERWISE SPECIFIED
A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) NO JEDEC REFERENCE AS OF
   FEBRUARY 2006
C) DIMENSIONING AND TOLERANCING PER
   ASME Y14.5M 1994

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